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Design of all-optical parity bit generator and checker using semiconductor material based devices

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In this communication, we are trying to design a new all-optical parity bit generator and parity checker operating in ultra high speed using four-wave mixing (FWM) and cross-polarization modulation (XPolM) phenomena in semiconductor optical amplifier (SOA). The hybrid encoding scheme with SOA is a very effective combination that helps to reduce the number of optical sources and also reduce the power requirement. As a result, the system hardware becomes simple and maintains the speed of operation 100 Gbit/sec. Two stages of the universal NOT gate using two SOA's compliments each other nicely. The first SOA with FWM non-linearity is the only process that is strictly transparent, including modulation-format and bit-rate transparency, and is capable of multiwavelength conversions. The second SOA shows XPolM non-linearity is used as a modulator and done the detection process efficiently using an optical polarizer at the output. The optical NOT gate is cascadable which helps to fabricate the design of our parity bit generator and checker devices. The performance of the optical device is verified using various numerical calculations and simulation techniques.

Keywords: Hybrid encoding, four-wave mixing (FWM), cross polarization modulation (XpolM), semiconductor optical amplifier (SOA), parity bit generator, parity checker.

Introduction

For ultrafast speed, less noise, quality communication optical devices are better than electrical and electronic devices. The optical parity bit generation and checking are one of the most important techniques in optical communication systems[1–6] for faithful data processing works. In this communication we use a hybrid encoded optical NOT gate as a general building block of our parity bit generator and checker circuits. This NOT gate (NG) was successfully used in our previous works[6–8]. The utility of even parity generator design was demonstrated in our previous work[7]. The newness in these designs is the use of four-wave mixing (FWM) and cross-polarization modulation (XpolM) phenomena of the semiconductor optical amplifier (SOA) at the same time. The circuit contains the utilities of both non-linear phenomena. The new hybrid encoding scheme also has the utility of frequency and intensity encoding at the same time[6–8]. The correction method is one of the most important techniques to maintain the originality of the data in an error-free manner. The parity generator circuit is used in the transmission station, adds an extra parity bit to the data depending on the number of highs and lows in the data. Receiving station uses the parity checking circuit to check whether a bit missing or extra unwanted bit is added. The state generates parity bits located in the sender station and the other one is a parity checker that checks produced parity bits and detects the errors if exists. This circuit used at the side of the receiver. Frequency encoding deals with high power laser sources and the intensity encoding faces loss dependence problem[9]. So the newly added hybrid encoding can remove the drawbacks of frequency and the other encoding techniques[14–16]. The hybrid encoding scheme reduces the number of signal gen-

erators and power supplies make the optical circuits simple. FWM in SOA is much more efficient than sum or difference frequency mixing in many non-linear medium[14–16] for a greater number of signal handling capacity. Semiconductor optical amplifiers (SOAs) have attracted a lot of researchers for its smaller size (~1 mm), low switching power requirement (<1 mW) and versatile application potential such as wavelength conversion, signal regeneration, optical switching as well as logic operations in the field of optical communications[15] at very high bit rates that cannot be handled by electronics. Polarization-independent FWM has received considerable attention recently[16–19]. One of the main advantages that FWM has over cross gain modulation (XGM) and cross-phase modulation (XPM) is due to the preservation of both amplitude and phase. FWM is strictly transparent when modulation formatting and bits rate are considered. So the non-linear effect can be efficiently used in multi-wavelength converters[17–23]. Another benefit of using FWM is that it is independent of modulation format due to it being a coherent process, unlike the other techniques, which are restricted to amplitude modulation formats. FWM can operate at high speed without degradation in the extinction ratio. The second part of the NOT gate is the intensity-dependent polarization modulator which can provide the facility of using both the inverted and non-inverted output signals as the design demands[24–29].

Working principle of the optical parity bit generator and checker

Hybrid encoding technique: The hybrid encoding technique is the hybridization of intensity and frequency encoding techniques. In the intensity encoding technique, two logical states 0 and 1 are represented by the absence of photon and the presence of photon. Then the detector will detect the intensity of lightwave which is lossy. In this hybrid encoding scheme, the presence of light (high state) is represented by the frequency of the optical signal (ν), like frequency encoding. The absence of light (low state) remains the same (0) as in the intensity encoding[8,9].

Working of NOT gate segment: Two basic mechanisms four-wave mixing and polarization rotation is utilized to implement the logic gates. In this communication degenerate, four-wave mixing is used. To analyze the performance in respect of input and output power, the four-wave mixing in SOA is modeled as a combination of lumped saturable gain, lumped third-order nonlinearity, and saturable amplified spontaneous noise (ASE) as used in the work by Lacey *et al.*[22].

Four-wavemixing: In this non-linear phenomenon numerous signals of nearly the same or different frequency interact into the medium of SOA to produce other frequencies. In general when a pump power with intensity I_1, is greater than the probe power with intensity I_2, spread in the SOA, then new frequencies will be generated transforming light with frequency ($2\nu - \nu_s$) and idler light with frequency ($2\nu_s - \nu$)]. The intensity of the transforming light and idler light will be proportional to $I_1^2I_2$ and $I_1I_2^2$ respectively[16]. Now since $I_1 > I_2$, therefore transforming light intensity is greater than idler light. So this transformation light with frequency ($2\nu - \nu_s$)can be used as the pump wave of the next major section, the SOA Polarization Rotator (SOA P.ROT) after crossing an opticalfilter (F_1). This filter passes only the ($2\nu - \nu_s$), frequency and plays an important role. The whole process will be shown in the figure below (Fig. 1).

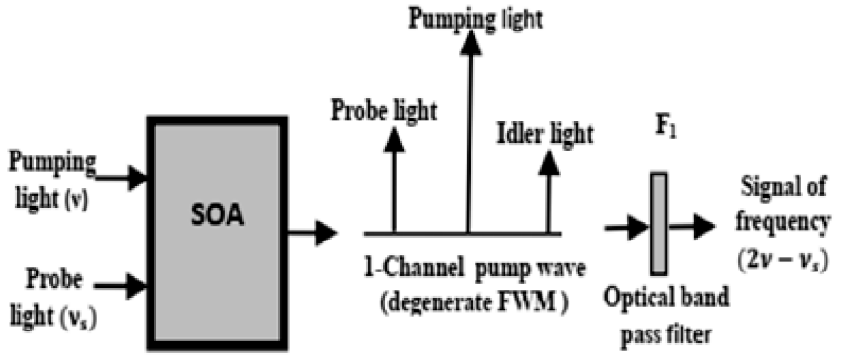

Fig. 1. Four-wave mixing (FWM) in SOA.

Table 1. Parameters used in the simulation for four-wave mixing in SOA[14]

Parameters	Values
a, b (experimentally determined constants)	0.88, 0.76
γ, γ' (experimentally determined constants)	11 dB, –40 dB/0.1 nm
R (Relative conversion efficiency function)	–39 dB

Polarization modulator: The cross-polarization modulation (XPolM) phenomenon in SOA (SOA P. ROT) with an optical polarizer combinedly produces a switching effect[8]. XpolM is a special type of non-linear polarization rotation (NPR) effect where a high intense pump beam modulates the state of polarization of the low-intensity probe beam. The modulation happens as a combinational effect of gain compression and birefringence[24–29] imposed on the transverse electric (TE) and transverse magnetic (TM) components of the probe signal. An external polarization beam splitter (PBS) provides two different ports for the polarization rotated and unrotated probe in the presence and absence of pump signals respectively. A polarization analyzer can be used to select and pass an optical signal with a particular state of polarization. Then the whole arrangement works like a polarization rotator or half-wave plate.

This design has great potential to offer wavelength conversions with high extinction ratios[24].

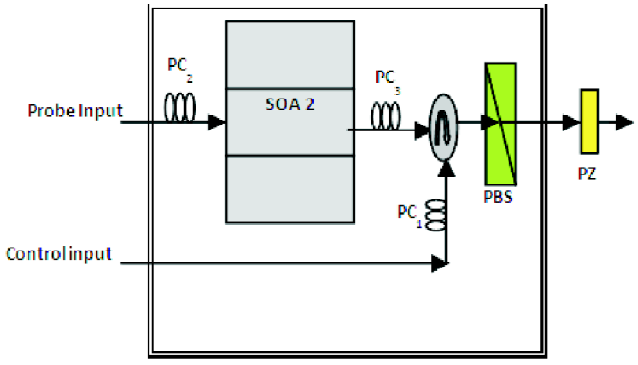

Fig. 2. SOA polarization rotator (SOA P. Rot).

The theoretical model behind the simulation works

Theory of four-wave mixing (FWM): In this theory, non-birefringent bulk SOA is used to neglect the polarization sensitivity in SOA FWM (Fig. 3). The FWM in SOA is used to provide wavelength conversion (WC) effect to support the co-propagation effect in the next polarization rotator section. The output power of this WC is given by,

$$P_{WC} = SL_1L_2G^3R \quad (1)$$

where S - input probe power, L_1 and L_2 - the power of orthogonally polarized components of pump signal, G-SOA's gain; R - relative conversion efficiency[22,23].

For, components with equal power we can write $L_1 = L_2 = L$. Therefore,

$$P_{WC} = SL^2G^3R \quad (2)$$

The optical gain (G) can be expressed as

$$G = a(P_I)^{-\gamma} \quad (3)$$

where, a,γ - experimental constants[22] given in Table 4, P_I - total input signal power given by,

$$P_I = S + 2L \quad (4)$$

The output P_{WC} is used as the power of the control signal in the next section which introduces the intensity-dependent polarization rotation effect in SOA2.

Table 2. SOA (FWM) parameters used for simulation

Parameters	Value
Device length	1 mm
Gain cross section	10.2×10^{-20} m^2
Line width enhancement factor	3
Mode confinement factor	0.47
Device current	170–200 mA
Carrier density at transparency	2.7×10^{23} m^{-3}
Input power	0.5 mW

Theory of intensity-dependent cross-polarization modulation: Another principle behind the operation of the logic gates proposed in this communication is the polarization rotation in SOA in the counter-propagating scheme. The details of the theory can be found in the work by Dorren *et al.*[28], based on the rate equation model. Inside SOA, the two components TE and TM modes, experience difference in gain results in cross-polarization modulation is the heart of the polarization rotator switch (SOA P. ROT). In Fig. 2, a signal modulator (SOA P. Rot) based on polarization rotation is shown which consists of an SOA, a band-pass filter, BPS, a polarization beam splitter (PBS), a circulator and three po-

larization controller PC_1, PC_2, and PC_3. The output of the polarization rotation switch-based frequency converter is given by,

$$P_{PR} = P^{TE} + P^{TM} + 2\sqrt{(P^{TE}.P^{TM})} \cos(\theta + \Phi) \quad (5)$$

$$\text{where } P^{TE} = P_{in}{}^{TE}[\cos^2\beta \cos^2\delta]G^{TE} \quad (6)$$

and

$$P^{TM} = P_{in}{}^{TM}[\sin^2\beta \sin^2\delta]G^{TM} \quad (7)$$

where $P_{in}{}^{TE}$, $P_{in}{}^{TM}$ - power of transverse electric and transverse magnetic component of probe signal, θ - phase change in presence of control signal, Φ - initial phase difference between TE and TM components, β - the angle of incidence of the probe signal with SOA layers, δ - the angle between PBS axis and SOA layer orientation.

The switching energy (~ 0.5 mW) of the polarization rotator is reported by Zhang *et al.*[29]. In this model[29] they have considered $\delta \sim 62°$, $\beta \sim 43°$ for an SOA biasing current 160 mA. In this paper, we have considered $\delta \sim \beta \sim 45°$ and we get a similar result. The parameters of the SOA polarization rotator is given in Table 3.

Table 3. SOA parameters for the NPR effect

Parameters	Value
Confinement factor	0.2
Model loss in TE mode	0.27 ps^{-1}
Model loss in TM mode	0.27 ps^{-1}
Gain coefficient	7.0×10^{-9} ps^{-1}
Saturation energy	750 fJ
Electric current	160 mA
SOA length	800 μm

The circuit operation of the basic building block

We have used the NOT gate (NG) as the basic building block of the design of parity bit generator and checker.We have already fabricated one of the universal logic gates i.e. NOT gate in our previous work[7] and is used again in this communication explained below.

The proposal of experimental design is based on a pump-probe approach, where the polarization of a CW beam is modulated by a high-intensity pulsed pump beam. The first SOA produces different signals of frequency ν, ν_s, $(2\nu - \nu_s)$, $(2\nu + \nu_s)$, etc. as a result of four waves mixing. Filter F_1 passes the signal with $(2\nu - \nu_s)$. Now, this high-intensity signal is coupled with another low intensity prove signal of frequency ν, in SOA P. ROT. Then the system rotates the plane of polarization of the probe signal in the presence of the pump signal. The polarizer after the nonlinear medium (SOA P.ROT.) of the light to block the transmission of polarization rotated signal.

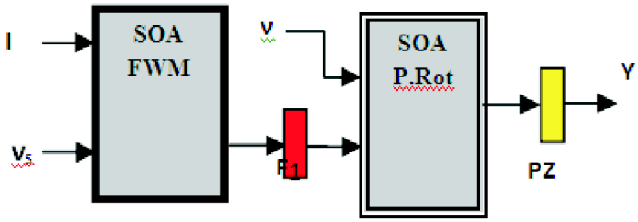

Fig. 3. NOT gate (NG).

Case 1: When A = 0, pump signal of SOA P. ROT is absent and the state of polarization of the probe signal remains unchanged is passing by the polarizer. So the output Y = ν.

Case 2: When A = ν, pump signal of SOA P. ROT is present and the state of polarization of the probe signal is rotated and is blocked by the polarizer. So the output Y = 0.

Table 4. Truth table the basic switch

Case	Input (I)	Output (Y)
1	0	ν
2	ν	0

The circuit operation of the XGS block

The XGS block is made off the 4 NGS just to maintain the simplicity of the design and the power symmetry. The operation of the XOR gate or the XGS block (Fig. 4) is shown in Table 5.

Case 1 and 4: When I1 = I2 = 0 or ν both the NG 3 and 4 outputs are 0. So the XGS output is 0.

Case 2 and 3: when, I1 = 0, I2 = ν or I1 = ν, I2 = 0, then either of the output of NG 3 or 4 is present and the final XGS output is ν.

The circuit operation of parity bit generator

A parity bit generator for a 3-bit message can be designed (Fig. 5) using the XGS blocks the operation is shown in the truth Table 6. For even parity, the parity bit P_E is generated to make the number of 1 or ν's even (including P_E) and for odd

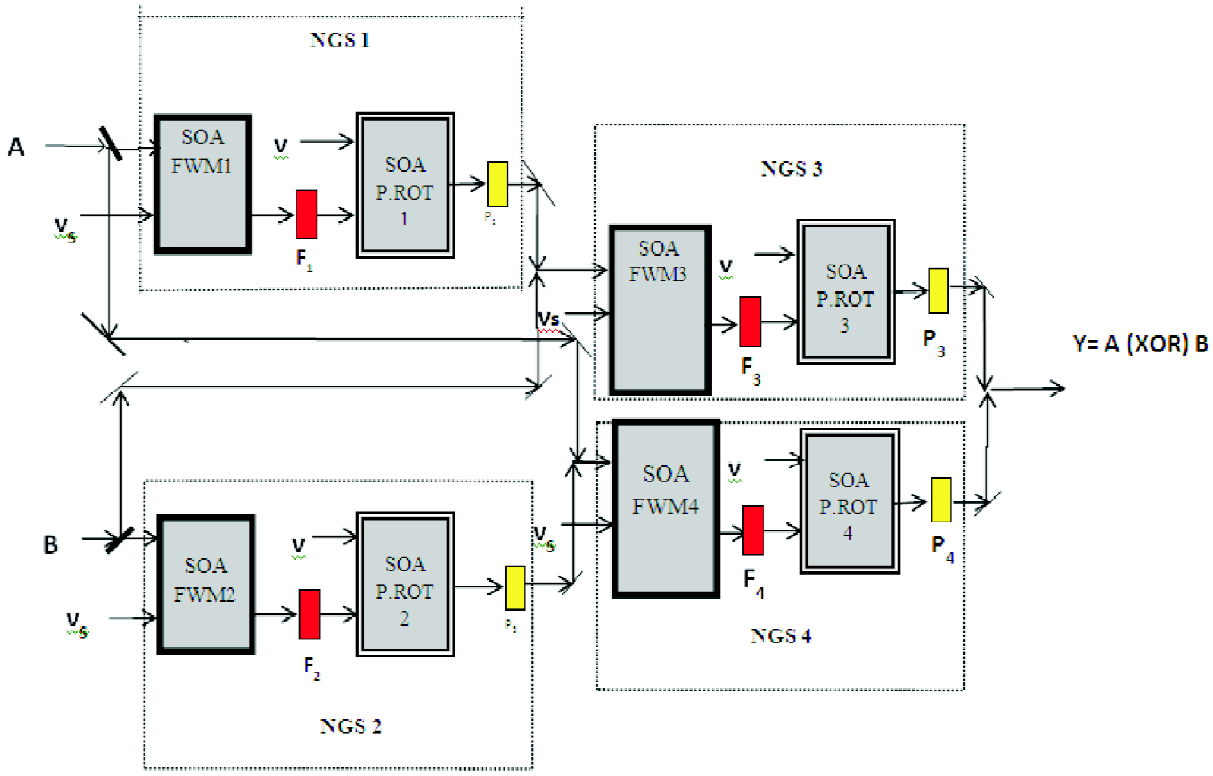

Fig. 4. XOR gate segment (XGS).

Table 5. The truth table for the XGS block

Case	Input 1 (I1)	Input 2 (I2)	Output (Y)
1	0	0	0
2	0	ν	ν
3	ν	0	ν
4	ν	ν	0

parity, the parity bit P_O is generated to make the number of 1or ν's odd (including P_O).

When A = B = 0, the output of XGS1 is 0. In these cases, if C = 0 then $P_E = Y_2 = 0$ and $P_O = \nu$. If C = ν, then output $P_E = Y_2 = \nu$ and $P_O = 0$.

When A = B = ν, the output of XGS1 is 0. In this case if C = 0 then $P_E = Y_2 = 0$ and $P_O = \nu$. If C = ν, then output $P_E = Y_2 = \nu$ and $P_O = 0$.

When either A = 0, B = ν, or A = ν, B = 0, the output of XGS1 is ν. In this case if C = 0 then $P_E = Y_2 = \nu$ and $P_O = 0$. If C = ν then output $P_E = Y_2 = 0$ and $P_O = \nu$.

Then this extra parity bit is developed and is added to the

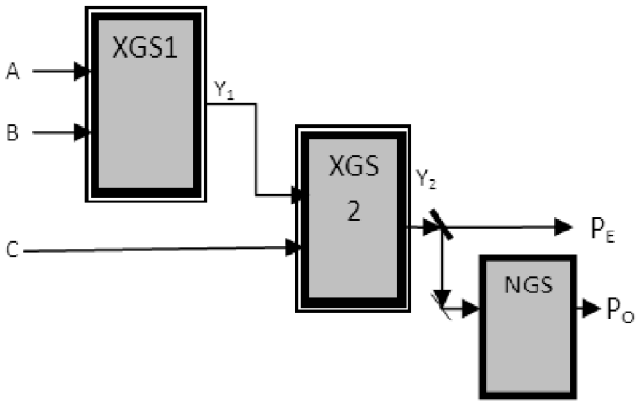

Fig. 5. Parity bit (even and odd) generator for 3-bit message.

original data which signifies the number of high states in the data stream. This parity is checked at the parity bit checker section discussed in the next section.

Working of the parity bit checker

The parity checker counts the number of 1's or ν's in the instructional code including the parity bit (P). An even parity

Table 6. The truth table for the parity bit generator

3-bit message				Parity bit generator (P)	
				Even	Odd
A	B	Y_1	C	P_E	P_O
0	0	0	0	0	ν
0	0	0	ν	ν	0
0	ν	ν	0	ν	0
0	ν	ν	ν	0	ν
ν	0	ν	0	ν	0
ν	0	ν	ν	0	ν
ν	ν	0	0	0	ν
ν	ν	0	ν	ν	0

checker shows "0" at the output for the presence of an even number of 1's or high states at the input data stream. Similarly, the design shows "1" at the output in the presence of an odd number of 1's at the input. The work of the odd parity bit checker is just the opposite to the even parity bit checker, means that it will show "0" at the output for the presence of an odd number of 1's at the coded input signal and "1" at the output for the presence of even number of 1's at the input signal. So our 3-bit input data stream now consists of 4 bits including the extra parity bit in LSB position and the 4-bit data stream is checked by the parity checker design at the receiving station just to verify the originality of the incoming information.

The first two-bit (A, B) of the input message is connected to the input port of XGS1 and the next two bits (C, P) are connected to the input port of XGS2. The outputs (Y_1 and Y_2) of these two XOR gate segments are connected to the input port of XGS3 as per Figs. 7 and 8. The output of this even and odd parity checker for all possible combinations of inputs is shown in Table 7. The complete design of our proposed parity checker is shown in Fig. 6.

When A = B = 0 or ν, C = P = 0 or ν, output $Y_1 = Y_2 = 0$ and final output $C_{EP} = 0$, $C_{OP} = \nu$.

When A ≠ B (one is 0 another is ν), C = P = 0 or ν, output $Y_1 = \nu$, $Y_2 = 0$, and final output $C_{EP} = \nu$, $C_{OP} = 0$.

When, A ≠ B (one is 0 another is ν), C ≠ P (one is 0 another is ν), output $Y_1 = Y_2 = \nu$, and the final outputs $C_{EP} = 0$, $C_{OP} = \nu$.

When, A = B = C = P = 0 or ν, output $Y_1 = Y_2 = 0$ and the final outputs $C_{EP} = 0$, $C_{OP} = \nu$.

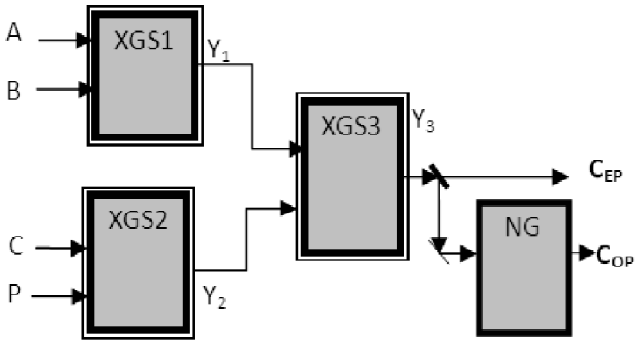

Fig. 6. Parity bit (even and odd) checker for 3 bit message.

When A = B = 0 or ν, C ≠ P (one is 0 another is ν), output $Y_1 = 0$, $Y_2 = \nu$, and final output $C_{EP} = \nu$, $C_{OP} = 0$.

Table 7. The truth table of the parity checker

A	B	C	P	Y_1	Y_2	Y_3	
						C_{EP} (even)	C_{OP} (odd)
0	0	0	0	0	0	0	ν
0	0	0	ν	0	ν	ν	0
0	0	ν	0	0	ν	ν	0
0	0	ν	ν	0	0	0	ν
0	ν	0	0	ν	0	ν	0
0	ν	0	ν	ν	ν	0	ν
0	ν	ν	0	ν	ν	0	ν
0	ν	ν	ν	ν	0	ν	0
ν	0	0	0	ν	0	ν	0
ν	0	0	ν	ν	ν	0	ν
ν	0	ν	0	ν	ν	0	ν
ν	0	ν	ν	ν	0	ν	0
ν	ν	0	0	0	0	0	ν
ν	ν	0	ν	0	ν	ν	0

Result of the simulation works and discussion

The performance of our proposed parity bit generator and parity checker is verified taking a 4-bit input data message (including P bit) using simulation methods and the results are shown herein. The performance of these designs is verified with some simulation work using MATLAB and is described in this section. The parameters used in simulation purposes are already given in Tables 1 and 2 for FWM and NPR effects respectively. We have taken a CW type probe

(~0.023 mW) and a Gaussian type pump or data signal (~0.5 mW^{-1} – 1 mW).

We have used the unrotated probe signal of the basic switch or the NOT gate. This signal is emitted from the inverting port of the switch where the power of the signal decreases with the increase in pump power. As a result, we need very low input signal power (<0.1 mW) to get the maximum output power for each switch (Fig. 7).

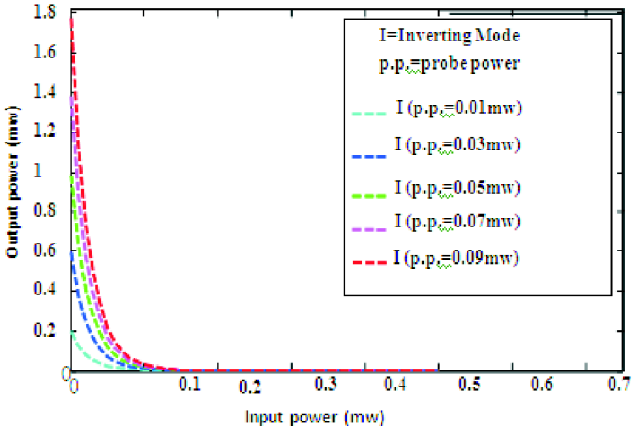

Fig. 7. Variation of probe output with input power.

The effect of amplified spontaneous (ASE) noise effect is considered in our calculation. This noise effect increases with the increase in injection current in SOA. Some performance-related parameters like Quality factor (Q), Extinction Ratio (ER), and Contrast Ratio (CR) for the proposed design of parity bit generator and checker are calculated and plotted, using standard mathematical formula[24] (eqs. (8)–(10)) with MATLAB programming.

$$Q = [(P^1_{mean} - P^0_{mean})/(\sigma^1 + \sigma^0)] \quad (8)$$

$$ER = 10.\log (P^1_{min}/P^0_{max}) \quad (9)$$

and

$$CR = 10.\log (P^1_{mean}/P^0_{mean}) \quad (10)$$

where P^1_{mean} - average power of the high state, P^0_{mean} - average power of the low state, σ^1 - standard deviation of high state, σ^0 - standard deviation of low state, P^1_{min} - minimum power among all the high output states, P^0_{max} - maximum power among all the low output states.

These matrices depend on several factors like the structure parameters, bias current, and the input signal power. In this communication, we are taking constant values of parameters for the good performance of the proposed design.

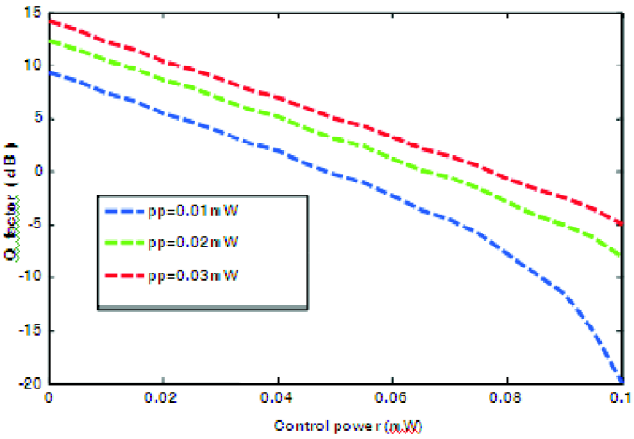

Fig. 8a. Variation of Q factor with control power.

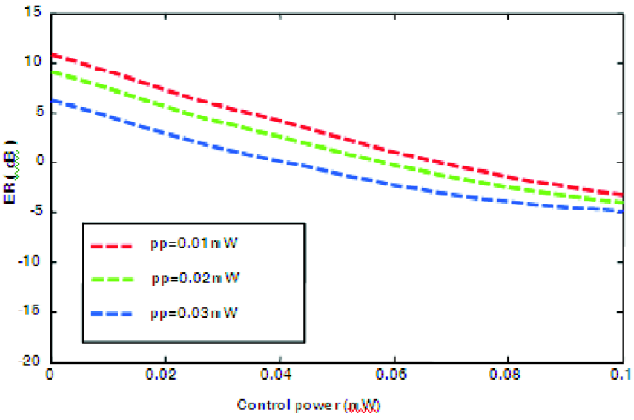

Fig. 8b. Variation of ER with control power.

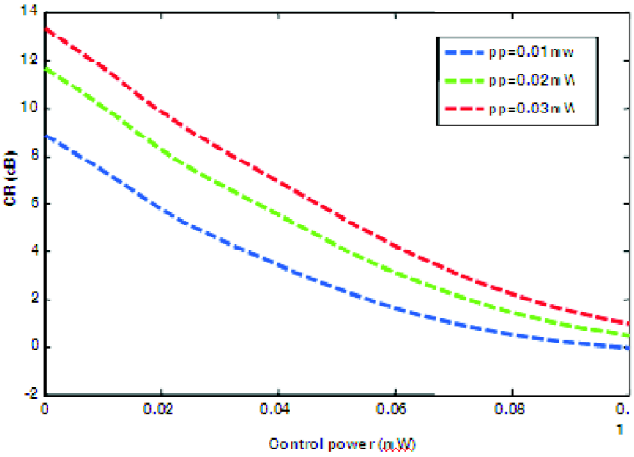

Fig. 8c. Variation of CR with control power.

Figs. 8a, b and c shows, the variation of Q factor, extinction ratio (ER), and contrast ratio (CR) with control and probe power respectively. Due to the inverting mode of operation of the design, each curve decreases with an increase in control power. This happens because of the blocking effect of the polarizer used in the output when the plane of polarization is changed in presence of a control signal and this effect is more or less unchanged in the design of even and odd parity generator and checker devices.

Input data stream used in the simulation (A, B and C)

The parity bit is generated using the input bit pattern of signal A = [1(ν), 0, 1(ν), 0, 1(ν)] in Fig. 9a , signal B = [0, 1(ν), 0, 1(ν), 0] in Fig. 9b, signal C = [0, 0, 1(ν), 0, 1(ν)] in Fig. 9c.

The outputs of the parity bit generator are given by, output P_E = [1(ν), 1(ν), 0, 1(ν), 0] in Fig. 9d and output P_o = [0, 0, 1(ν), 0, 1(ν)] in Fig. 9e.

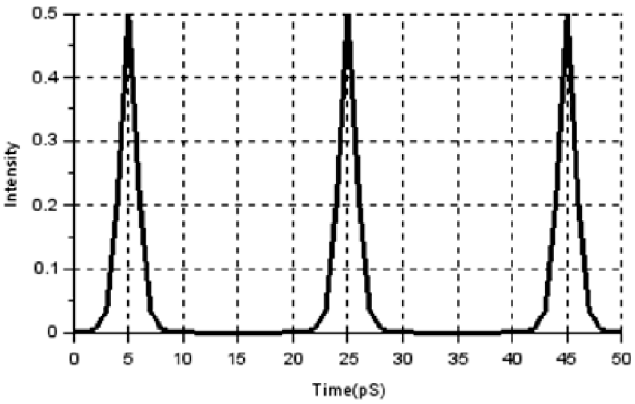

Fig. 9a. Input A.

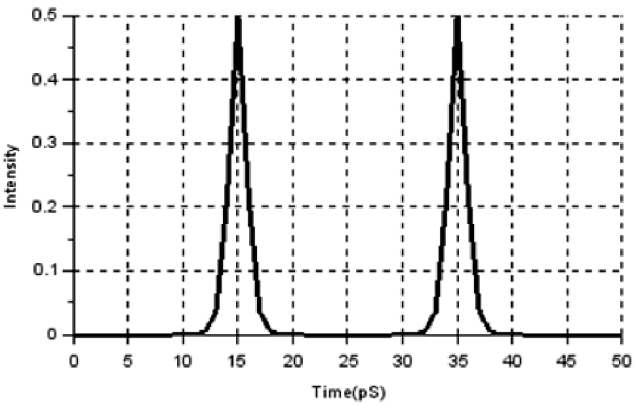

Fig. 9b. Input B.

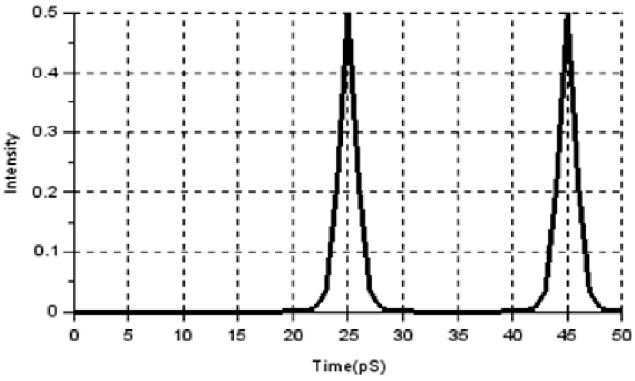

Fig. 9c. Input C.

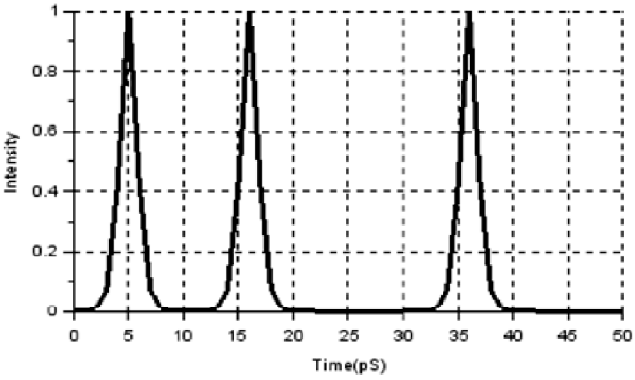

Fig. 9d. Output P_E.

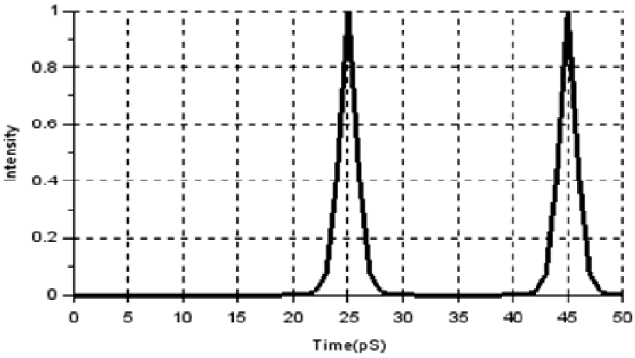

Fig. 9e. Output P_O.

Now to check the parity in the 4-bit input data stream (A, B, C, P) we have two sets of possible combination of input bits set I = (1001, 0101, 1010, 0101, 1010) using even party bit P_E and set II = (1000, 0100, 1011, 0100, 1011) (1 stand for ν) using odd parity bit P_O.

The even parity checker shows 0 and 1 at the output

when the number of 1's is even and odd in the input data stream. So the output C_{EP} shows 0 (Fig. 9f) and 1(ν) (Fig. 9g).

The odd-parity checker shows 0 and 1 at the output when the number of 1's is odd and even in the input data stream. So the output C_{OP} shows 1(ν) (Fig. 9h) and 0 (Fig. 9(i)).

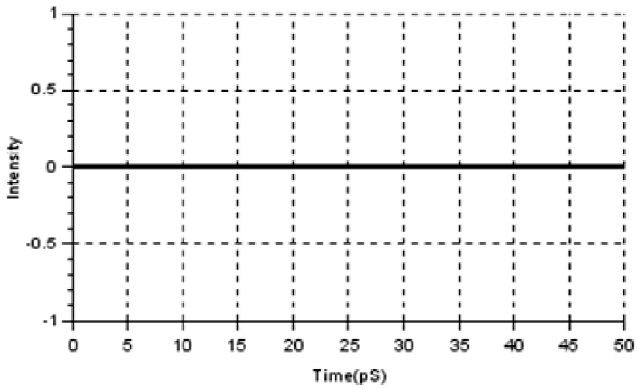

Fig. 9f. Output C_{EP} for the set I.

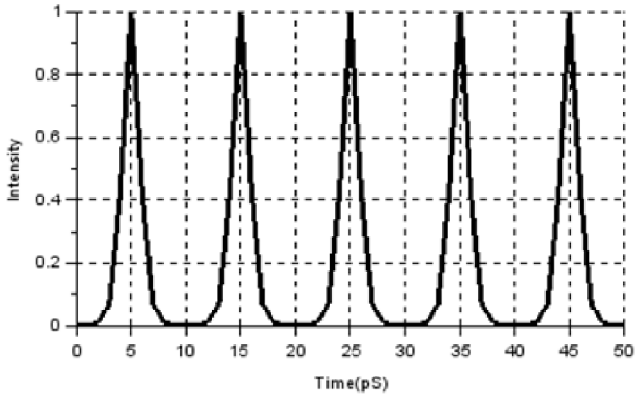

Fig. 9g. Output C_{EP} for the set II.

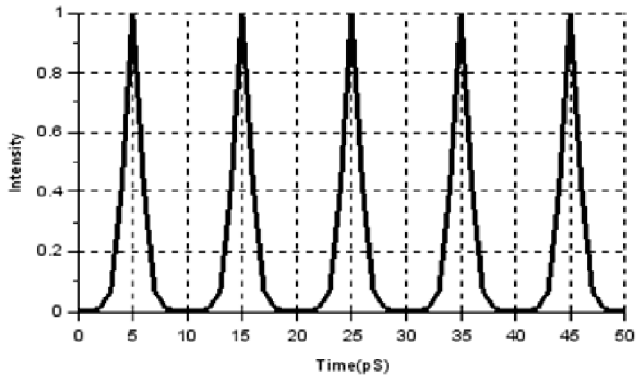

Fig. 9h. Output C_{OP} for the set I.

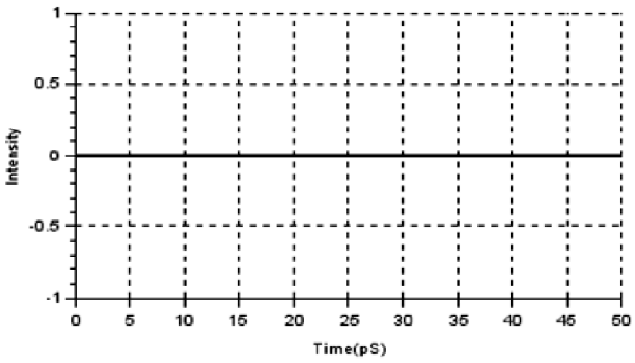

Fig. 9(i). Output C_{OP} for the set II

Conclusions

The consideration of a hybrid encoding scheme is based on the frequency which reduces the signal distortion possibility and hardware complexity. The small size of the SOA device (~1 mm) with a small active region and its higher dielectric constant means that the required peak power is much lower (<1 mW) than the highly nonlinear fibers (>100 mW). The optical logic gates we use are cascadable and can operate at high speed (100 Gbps) without degradation in the extinction ratio. The quality factor of our proposed design is good enough (>10 dB) for practical use. So parity generator and checker for higher bits data signals, working with ultra-high-speed can be fabricated. The performance of the design may be affected due to the heating effect. Some problems may arise in controlling the polarization of signals. But the problem is lesser than Optical Fibre Amplifiers (OFA's) and can be minimized. Using this scheme other complicated higher-order optical computational devices like the adder, flip-flop, comparator, counter, etc. can be fabricated.

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