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Impact of annealing process on electrical characteristics of Ni Schottky rectifiers fabricated on p-type Si

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In this work, the electrical parameters of Ni/p-Si SBDs have been investigated using I-V and C-V techniques as a function of annealing temperature. The experimental analysis revealed that the SBHs of the Ni/p-Si SDs are 0.53 eV (I-V) and 0.54 eV (Norde) for as-deposited, 0.56 eV (I-V) and 0.58 eV (Norde) for 300°C, 0.58 eV (I-V) and 0.59 eV (Norde) for 400°C, and 0.50 eV (I-V) and 0.49 eV (Norde) for 500°C, respectively. By performing C-V measurements for the Ni/p-Si SBDs, the SBH values were found to be in the range 0.64–0.59 eV for the as-deposited and 500°C annealed samples, respectively. Further, interface state density (N_{SS}) values of Ni/p-Si SD is estimated and is noticed that the N_{SS} values decreases up to 400°C annealing temperature and slightly increases after annealing at 500°C.

Keywords: Schottky diode, ideality factor, MS structure, Schottky barrier height, interface state density.

Introduction

Metal-Semiconductor (MS) Schottky barrier diodes (SBDs) are essential building blocks and most extensively used in electronics industry. Recently, because of their thriving operation in electronic devices[1,2], there has been promising significance in the field of SDs. These devices have been studied broadly but an adequate understanding of current transport mechanism that exists at the MS interface has not been understood clearly so far. Generally, the electronic parameters of a SD are described by its Schottky barrier height (SBH), series resistance (R_s) and ideality factor (IF). These parameters give valuable information thoroughly and reveal the nature of the device and barrier formation at the interface. However, the unintentionally formed oxide layer at the MS interface in the laboratory environment plays an important role and can affect device performance/reliability[3]. Furthermore, the calculated SBHs evaluated from I-V and C-V techniques vary with each other and the reasons were explained in references[4,5]. As a result, the development of high-quality Schottky contacts for all semiconductors devices with superior thermal stability at high temperatures is yet a challenging task.

In this work, we have analyzed the electrical parameters of Ni/p-Si SDs at different annealing temperatures ranging from 300–500°C. The barrier parameters controlling the device performance such as SBH, ideality factor (IF) and series resistance (R_s) are evaluated by current-voltage (I-V) and capacitance-voltage (I-V) techniques at different annealing temperatures ranging from 300–500°C. Furthermore, we analyzed the interface sate density (N_{SS}) values for the Ni/p-Si SBDs at different annealing temperatures.

Device fabrication:

The Ni/p-Si MS SBDs were prepared on p-Si substrate. Prior to the fabrication procedure, the wafer was cleaned in trichloroethylene, acetone and dipped in H_2O:HF (10:1) solutions for a period of five minutes in an ultrasonicator. Then the samples were dipped in de-ionized water and blown with

high-purity nitrogen. After these steps the samples were instantly transferred into electron-beam evaporation system and high purity Al (200 nm) was thermally evaporated on to the entire rough side of Si under the vacuum of 6×10^{-5} mbar. To form low resistivity Ohmic contact, the Al deposited samples were annealed at 450°C for 5 min in N_2 atmosphere. After the formation of Ohmic contacts, the high purity Ni Schottky dots with 0.7 mm diameter and 70 nm thickness was deposited on smooth surface of p-Si wafer using photolithography method. Fig. 1 demonstrate the schematic illustration of the fabricated Ni/p-Si SBD. To ensure thermal stability issue of prepared Ni/p-Si/Al SBDs, the as-deposited samples were annealed at 300, 400 and 500°C for 1 min in N_2 ambient. The I-V and C-V measurements of Ni/p-Si SBDs were performed using SMU Keithley source (Model: 236) and LCR meter, respectively.

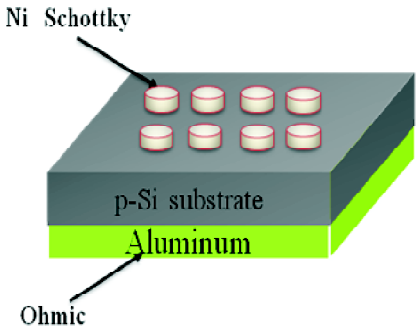

Fig. 1. Schematic diagram of the fabricated Ni/p-Si SBD.

Results and discussion

Fig. 2 demonstrates the I-V characteristics of Ni/p-Si at different annealing temperatures ranging from 300 to 500°C.

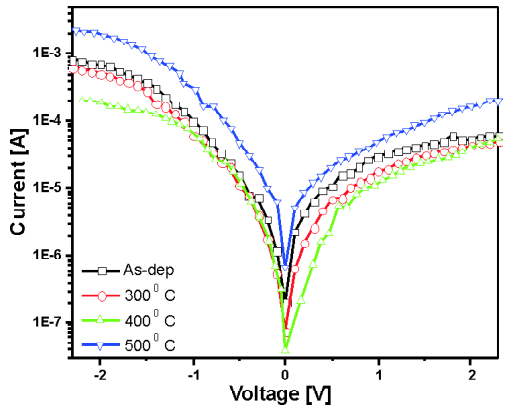

Fig. 2. Plot of current-voltage (I-V) characteristics for Ni/p-Si SBD at various annealing temperatures.

The leakage currents of as-deposited, 300, 400 and 500°C Ni/p-Si SBDs were found to be 3.7×10^{-4} A, 2.73×10^{-4} A, 1.31×10^{-4} A and 1.03×10^{-3} A at –1.5 V, respectively. The 500°C annealed sample exhibited a decrease in SBH with a corresponding increase in reverse leakage current. With the help of thermionic emission (TE) model[6], the BH (ϕ) and ideality factor (n) can be found from linear fit to the linear section of forward-bias ln I-V curves and is expressed as

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(\frac{qV}{nkT}\right)\right] \quad (1)$$

where

$$I_0 = AA^{**}T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \quad (2)$$

Here, 'I_0' is the saturation current, 'A' is area of Schottky diode, 'q' is electronic charge, 'T' is absolute temperature in Kelvin and SBH can be estimated using the equation

$$\phi_b = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_0}\right) \quad (3)$$

Here A^{**} is effective Richardson constant (32 A cm^{-2} K^{-2} for p-Si). The estimated BH and IF values of Ni/p-Si SD was found to be 0.53 eV, 1.45 (as-deposited), 0.56 eV, 1.21 (annealed at 300°C), 0.58 eV, 1.13 (annealed at 400°C) and 0.50 eV, 1.54 (annealed at 500°C), respectively. Experimental results indicated that all the samples exhibited 'n' values which are larger than one. The reason for these larger values of 'n' is attributed to the presence of potential drop and laterally inhomogeneous barriers that exist at the MS interface[7]. To find out reliable barrier height ϕ_b, Norde[8] proposed an alternative method. The Norde function can be represented as

$$F(V) = \frac{v}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^{**}T^2}\right) \quad (4)$$

where 'γ' is dimensionless integer whose value is greater than 'n', $I(V)$ is current obtained from Fig. 3. Thus, the effective SBH can be written as

$$\phi_b = F(V_{min}) + \frac{v_{min}}{y} - \frac{kT}{q} \quad (5)$$

where $F(V_{min})$ is the minimum value of $F(V)$ and V_{min} is the subsequent voltage. The series resistance (R_s) value is calculated using the equation

$$R_s = \frac{kT\,(y-n)}{q^{I}} \tag{6}$$

where '*I*' is the current at which *F*(*V*) is minimum. From Fig. 3, ϕ_b and R_s are found to be 0.54 eV and 9.5 kΩ for as-deposited, 0.58 eV and 4.7 kΩ for 300°C, 0.59 eV and 2.7 kΩ for 400°C, 0.49 eV and 13.2 kΩ for 500°C respectively. Also, the SBH (ϕ_b) calculated from I-V and Norde methods are in excellent agreement with respect to each other.

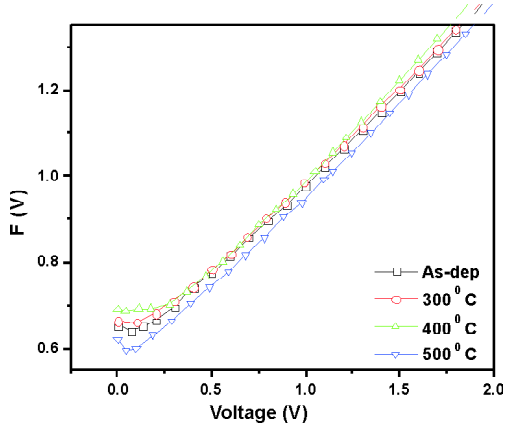

Fig. 3. *F*(*V*) versus *V* curves for Ni/p-Si SBDs at various annealing temperatures.

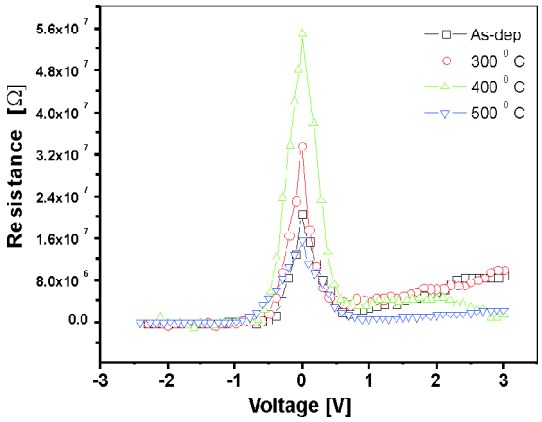

Fig. 4. The voltage-dependent diode resistance of the Ni/p-Si SBD at different annealing temperatures.

As shown in Fig. 4, the main important parameters such as series resistance (R_S) and shunt resistant (R_{Sh}) are determined from the diode resistance ($R_i = \partial V/\partial I$) versus bias-voltage (*V*) plot for the Ni/p-Si SBD at various annealing temperatures. From Fig. 4, the extracted R_S and R_{Sh} values are estimated to be 8 MΩ and 20 MΩ for as-deposited, 9 MΩ and 33 MΩ for 300°C, 1 MΩ and 46 MΩ for 400°C, 2 MΩ and 15 MΩ for 500°C samples respectively. This analysis confirmed that the sample annealed at 400°C has shown superior electrical characteristics when compared to other samples.

The $1/C^2$-*V* characteristics of Ni/p-Si SBDs were measured in the temperature range of 300–500°C and are shown in Fig. 5. The depletion layer capacitance in SBDs is represented as[9]

$$\frac{1}{C^2} = \frac{2\left(V_{bi} - \frac{kT}{q} - V\right)}{q\varepsilon_s N_a A^2} \tag{7}$$

where '*V*' is reverse-bias voltage, 'V_{bi}' is built-in potential, '*q*' is electronic charge, 'N_a' is doping concentration and ε_s is the dielectric constant of semiconductor. The built-in potential $\left(V_{bi} = V_0 + \frac{kT}{q}\right)$ is generally found by extrapolating C^{-2} versus *V* plot to X-axis. From C-V measurements, the BH can be calculated from

$$\phi_b = V_{bi} + V_p \tag{8}$$

where, $V_p = \frac{kT}{q} \ln\left(\frac{N_V}{N_A}\right)$

where 'N_v' is effective density of states in valance band and its value is 1.603×10^{18} cm^{-3} for p-Si at 300 K[10]. The evaluated BHs of Ni/p-Si SBDs using $1/C^2$ versus *V* curves of as-deposited and annealed samples at 300, 400 and 500°C are 0.64 eV, 0.69 eV, 0.71 eV and 0.59 eV, respectively. It is noticed that the calculated SBH values from C-V measure-

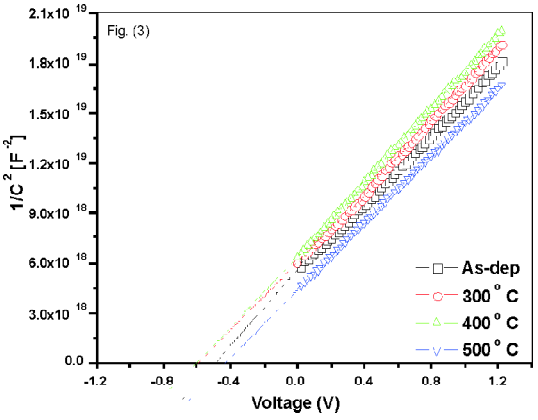

Fig. 5. $1/C^2$ versus *V* characteristics for Ni/p-Si SBDs.

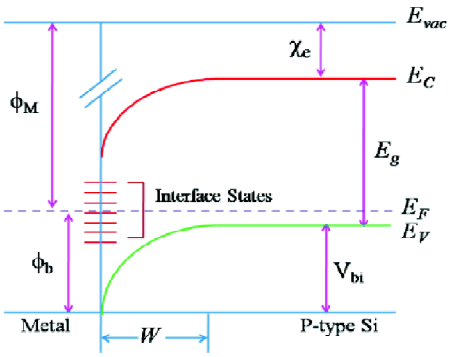

Fig. 6. Energy-level band diagram of the Ni/p-Si at various annealing temperatures. SBD with interfce states (where 'ϕ_b' is the Schottky barrier height, 'ϕ_m' is the work function of the metal, 'χ_e' is the semiconductor electron effinity, 'E_g' is the energy gap, 'V_{bi}' is the built-in pot- ential and 'W' is the depletion region width).

ments are higher than those attained from I-V measurements. This inconsistency observed in extracted SBH values may be because of the existence of lateral inhomogeneity that prevails at the MS interface[11]. One more possible reason for this discrepancy may be because of the presence of excess capacitance at the interfacial layer owing to deep level traps in the semiconductor[11] and/or stacking faults that present on the Si semiconductor[9].

The energy-level band diagram of the Ni/p-Si SBD with interface states after the metal contact has been made is shown in Fig. 6. As proposed by Card and Rhodercik[12], for a real MS SD having interface states in equilibrium with the semiconductor, the 'n' becomes greater than one and is represented as

$$n(v) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + q.N_{ss}\right] \quad (9)$$

where 'W_D' is the space charge region width, 'N_{ss}' is the interface states density, δ, ε_s and ε_i are thickness of the interfacial layer, permittivity of semiconductor and interfacial layer, respectively. The 'N_{ss}' can be evaluated by substituting the voltage-dependent $n(V)$ can be expressed as $n(v) = V/(kT/q)$ ln (I/I_s)[13]. The evaluated N_{ss} curves are represented in Fig. 7, using the following equation

$$N_{ss} = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \quad (10)$$

In case of p-type semiconductor, the energy of the interface states, E_{ss} with respect to top of the valence band at the semiconductor surface is represented as[14,15]

$$E_{ss} - E_V = q\,(\phi_b - V) \quad (11)$$

The effective barrier height 'ϕ_s' is related to the ideality factor $n(V)$ by

$$\phi_\varepsilon = \phi_b + \left(1 - \frac{1}{n(v)}\right)V \quad (12)$$

The energy density distribution of interface states in equilibrium with the semiconductor was extracted from the data of the forward bias I-V. The calculated values of N_{ss} at various annealing temperatures are found to be 3.0236×10^{14} eV^{-1} cm^{-2} (E_V –0.60 eV) for as-deposited, 1.9764×10^{15} eV^{-1} cm^{-2} (E_V –0.66 eV), 3.3125×10^{15} eV^{-1} cm^{-2} (E_V –0.71 eV) and 1.5509×10^{15} eV^{-1} cm^{-2} (E_V –0.51 eV) for 300, 400 and 500°C annealed Ni/p-Si SBD, respectively. The experimental results demonstrated that the N_{ss} values decreases with increase in annealing temperature. On the basis of these findings, the variation of 'N_{ss}' with annealing temperature plays a substantial role in determining the electrical parameters of Ni/p-Si SBDs.

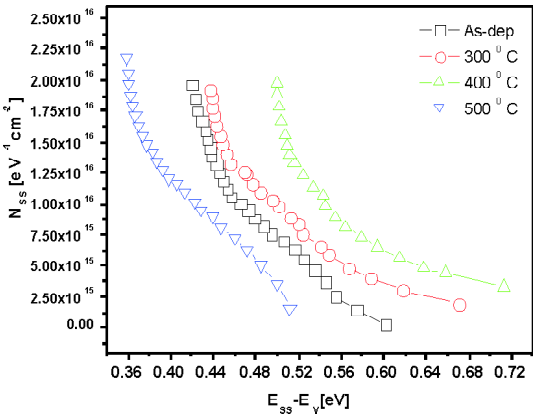

Fig. 7. The interface state energy distribution curves for the Ni/p-Si SBD as a function of annealing temperature.

Conclusions

The electrical characteristics of Ni/p-Si SBDs were examined by I-V and C-V measurements at various annealing temperatures. The values of the 'n', R_S and SBH were evaluated using forward-bias I-V characteristics. The SBH values estimated by means of the Norde function showed well agreement with the SBH values acquired from the I-V method. It is noticed that the values of SBHs extracted from C-V charac-

teristics for Ni/p-Si were particularly higher when compared to the values obtained from I-V technique. The reason for this difference observed in measured SBHs from I-V and C-V methods was successfully explained on the basis of inhomogeneities that prevailed at the MS interface. In conclusion, the analyzed experimental electrical properties such as SBH, R_S, R_{Sh} and N_{SS} for the Ni/p-Si SD are effectively explained with TE theory and were found to be strongly depending on annealing temperature.

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